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(12) United States Patent Ge et al.

(54) MANUFACTURE METHOD OF DUAL GATE OXIDE SEMICONDUCTOR TFT SUBSTRATE AND STRUCTURE THEREOF

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(56) References Cited

U.S. PATENT DOCUMENTS

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(57) ABSTRACT

The present invention provides a manufacture method of an oxide semiconductor TFT substrate and a structure thereof. The manufacture method of the dual gate oxide semiconductor TFT substrate utilizes the halftone mask to implement one photo process, which cannot only accomplish the patterning to the oxide semiconductor layer but also obtain the oxide conductor layer (52') with ion doping process, and the oxide conductor layer (52') is employed as being the pixel electrode of the LCD to replace the ITO pixel electrode in prior art; the method manufactures the source (81), the drain (82) and the top gate (71) at the same time with one photo process; the method implements patterning process to the passivation layer (8) and the top gate isolation layer (32) together with one photo process, to reduce the number of the photo processes to five for shortening the manufacture procedure, raising the production efficiency and lowering the production cost.

6 Claims, 5 Drawing Sheets



